REMARKS/ARGUMENTS

Status of Application

Claims 1-41 are pending in the present application. Claims 1-41 are rejected under 35 U.S.C. 102 (b). New claim 42 is added.

Rejection under 35 USC § 102(b)

Claims 1-41 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,100,173 (Gardner et al.). Applicants respectfully disagree.

Claim 1 recites a method of fabricating a gate electrode by providing a gate stack which includes a gate dielectric on a substrate and a gate layer over the gate dielectric. A metal layer is provided over the gate layer and a reaction consumes all of the gate layer and substantially all of the metal layer to form a resulting layer which serves as the gate electrode. The resulting gate electrode comprises a work function close to about a mid-gap of silicon band gap. Claim 10 recites a gate electrode having a work function close to about a mid-gap of silicon band gap formed from a first material and a metal in which the first material and substantially all of the metal have been consumed during reaction.

As for Claim 16, it recites a method for forming an integrated circuit in which a gate layer comprising an amorphous or polycrystalline material and a metal layer covering it are processed to cause a reaction in which all of the gate layer material and portions of the metal layer are consumed, wherein problems associated with inversion and agglomeration during formation of the transistor are reduced. Claim 41 recites an integrated circuit comprising a transistor having a gate electrode formed from an amorphous or polycrystalline first layer and a metal layer in which all of the first layer and substantially all of the metal layer have been

consumed during reaction with one another caused by annealing, wherein problems associated with inversion and agglomeration associated with formation of the transistor are reduced.

As for Gardner, it describes a silicide process which forms a silicide gate. The gate conductor comprises a polysilicon gate conductor and a refractory metal layer. An annealing step consumes a majority of the polysilicon gate conductor to convert it into the silicide gate conductor, with over 80% of the thickness of the polysilicon gate conductor being consumed by the metal silicide. It is even possible for more than 90% of the gate conductor to be consumed by the metal silicide. Applicants submit that this clearly suggests that some polysilicon gate conductor is not consumed. Therefore, Gardner fails to teach or suggest a gate electrode in which a gate layer is completely consumed, as required by claims 1, 10, 16 and 41.

Furthermore, by having a polysilicon layer in between the metal silicide layer and the gate dielectric, as taught by Gardner, the resulting gate electrode is a dual work function gate electrode. This is in contrast to the gate electrode of claims 1, 10 and 16, which requires a work function close to about the mid-gap of the silicon band gap. In addition, Gardner nowhere discusses reducing problems associated with inversion and agglomeration during gate formation, as required by claims 16 and 41. Applicants, in view of the arguments presented, submit that claims 1, 10, 16 and 41 are patentable over Gardner. Since claims 2-9, 11-15 and 17-40 are directly or indirectly dependent on claim 1, 10 or 16, these claims are also patentable over Gardner. Applicants therefore respectfully request withdrawal of the rejection to the claims based on 35 U.S.C. 102(b).

With respect to a newly added claim 42, it recites a method of fabricating a gate electrode by providing a gate stack which includes a gate dielectric on a substrate and a gate layer over the gate dielectric. A metal layer is provided over the gate layer and a reaction consumes substantially all of the gate and metal layers to form a resulting layer which serves as the gate

electrode. The gate electrode layer is in contact with the gate dielectric layer. Source/drain contacts are formed simultaneously with the gate electrode.

Gardner, in contrast, describes a dual silicide process which forms a gate conductor having a greater silicide thickness than silicide structures formed on source and drain junctions. The gate conductor is formed from a first anneal step. Subsequently, a second anneal step is conducted to form the junction silicides. *See* Gardner, col. 7, lines 2-16 and 37-46. Gardner nowhere teaches or suggests forming a gate electrode and source/drain contacts simultaneously, as required by claim 42. In fact, Gardner teaches that a two-step salicidation process is desirable to form a relatively thick gate silicide to avoid "junction spiking". *See* Gardner, col. 2, lines 39-56 and col. 7, lines 47-51. As such, Gardner teaches away from the invention as recited in claim 42. Applicants therefore submit that claim 42 is also patentable over Gardner.

Conclusion

In view of the foregoing, Applicants believe that all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this Application, please telephone the undersigned attorney at his number set out below.

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Respectfully submitted,

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